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| 10/683,641 | 10/09/2003 | Dwight W. Mattix | 030393 | 1207 |

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| EXAMINER | |
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| NORRIS, JEREMY C | |
| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/683,641 | MATTIX, DWIGHT W. | |
| | Examiner | Art Unit | |
| | Jeremy C. Norris | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,7,8,10,12-21 and 23-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,7,8,18-20 and 40-57* is/are allowed.

6)☒ Claim(s) *10,12-17,21 and 23-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10, 12, 14, 21, 23, and 26-39 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,972,382 B2 (Zollo).

Zollo discloses, referring primarily to figures 6A-D, an interlayer interconnection unit for a multi-layer PCB, comprising: a first capture pad (located in layer 67) having a corresponding first annular ring; a first via (through layer 68) having a first via inner end and a first via outer end, said first via outer end in contact with a corresponding one of said first capture pad and encircled by said corresponding first annular ring; at least one corresponding interstitial bridge pad (located in layer 69) having a first side and a second side, said first via inner end in contact with said first side of said corresponding interstitial bridge pad; a second via (77) having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said corresponding interstitial bridge pad; and a second capture pad (located in layer 6) having a corresponding second annular ring, said second via outer end in contact with a corresponding one of said second capture pad and encircled by said corresponding

second annular ring, wherein a first interstitial bridge pad of said at least one interstitial bridge pad lacks electrical connectivity to others of said at least one interstitial bridge pads, and wherein each one of said corresponding first annular ring, said first via, said corresponding interstitial bridge pad, said second via, and said corresponding second annular ring are coaxial with each other [claim 10], wherein said first via extends through a first dielectric layer (68), and said second via extends through a second dielectric layer (71) [claim 12], wherein: said multilayer PCB comprises an internal bridge layer (5), and said interstitial bridge pad is a component of said bridge layer [claim 14].

Similarly, Zollo discloses, a carrier for a multi-layer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including: a first metal layer (6); a first dielectric layer (71) disposed on said first metal layer; a bridge layer (5) disposed on said first dielectric layer; a second dielectric layer (68) disposed on said bridge layer; and a second metal layer disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads (located in layer 69), and wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said first metal layer by a corresponding first blind via (77) transversing said first dielectric layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said second metal layer by a corresponding second blind via transversing said second dielectric

layer (68), and wherein each of said plurality of interstitial bridge pads is coaxial in a z direction with said corresponding first blind via and with said corresponding second blind via, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [claim 21], wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads [claim 23], wherein: said first metal layer comprises a first signal layer of said PCB, and said second metal layer comprises a second signal layer of said PCB [claim 26], further comprising at least a third signal layer (3) laminated to said pseudo three-layer core [claim 27], wherein said carrier comprises 3 additional signal layers (1, 2, 3) laminated to said pseudo three-layer core [claim 28].

Additionally, Zollo discloses, a pseudo three-layer core for a printed circuit board (PCB), comprising: a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer (6) to a second metal layer (4), and comprises: a first dielectric layer (71) disposed on said first metal layer; a bridge layer (5) disposed on said first dielectric layer; and a second dielectric layer (68) disposed on said bridge layer, wherein said second metal layer is disposed on said second dielectric layer, and wherein at least one of said plurality of interlayer interconnection units an interstitial bridge pad located within said bridge layer (part of layer 69); a first blind via (77) extending from said first metal layer to a first side of said interstitial bridge pad; and a second blind via (located in layer 68) extending from said second metal layer to a second side of said interstitial bridge pad, wherein said

interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer, and wherein each of said plurality of interlayer interconnection units have said first blind via coaxial in the z direction with said second blind via [claim 29].

Furthermore, Zollo discloses, a multi-layer printed circuit board (PCB) comprising: a first signal layer (4); a second signal layer (6); a bridge layer (5) disposed between said first signal layer and said second signal layer; and a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer interconnection units comprises: a pair of opposed coaxial blind vias (located in layer 68 and via 77 respectively) transversing a first dielectric layer (71) and a second dielectric layer (68); and a bridge pad (located in layer 69) physically contacting said first and second dielectric layers, said bridge pad in electrical contact with said pair of blind vias, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer, and wherein each of said interlayer interconnection units include said pair of opposed coaxial blind vias with said bridge pad therebetween [claim 30], wherein: said bridge pad includes a first side and a second side; and wherein said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad [claim 31], further comprising

at least one additional dielectric layer (66) laminated to said first signal layer, and at least one additional signal layer (3) laminated to said at least one additional dielectric layer [claim 32].

Moreover, Zollo discloses, a multi-layer PCB, comprising: at least one pseudo three-layer core including: a first metal layer (6); a first dielectric layer (71) disposed on said first metal layer a bridge layer (5) disposed on said first dielectric layer; a second dielectric layer (69) disposed on said bridge layer; a second metal layer (4) disposed on said second dielectric layer; and a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises: an interstitial bridge pad (located in layer 69) having a first side and a second side; a first blind via (77) disposed on said first side of said interstitial bridge pad extending through said first dielectric layer; and a second blind via (located in layer 69) disposed on said second side of said interstitial bridge pad extending through said second dielectric layer, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer, and wherein each of said plurality of interlayer interconnection units have said first blind via coaxial in the z direction with said second blind via [claim 33], wherein each of said plurality of interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer [claim 34], wherein: each of said first metal layer and said second metal layer

comprises a signal layer, and said multilayer PCB further comprises at least one additional signal layer (3) laminated to said at least one pseudo three-layer core [claim 35], wherein said at least one pseudo three-layer core comprises a first pseudo three-layer core (4, 5, 6) and at least a second pseudo three-layer core (1, 2, 3) laminated to said first pseudo three-layer core [claim 36], wherein said multilayer PCB comprises 2 pseudo three-layer cores and 6 signal layers [claim 37].

In addition, Zollo discloses, a multilayer PCB, comprising: means for carrying a plurality of signal layers; and means for interconnecting at least two of said plurality of signal layers, wherein said carrying means comprises a pseudo three-layer core (4, 5, 6), wherein said pseudo three-layer core includes an internal bridge layer (5) that comprises a plurality of interstitial bridge pads (located in layer 69), a first dielectric layer (71), and a second dielectric layer (68), and wherein said interconnecting means comprises a pair of opposed blind vias disposed on either side of each of said plurality of interstitial bridge pads, said pair of opposed blind vias transversing said first and second dielectric layers, wherein each blind via of said pair of opposed blind vias are coaxially arranged in the z direction, and wherein each of said plurality of interstitial bridge pads is coaxial in a z direction with a corresponding one of said first blind via and with a corresponding one of said second blind via, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [claim 38], wherein: said bridge layer comprises an internal pseudo metal layer (69) disposed between a first dielectric

layer and a second dielectric layer, and wherein said interconnecting means is adapted for interconnecting said plurality of signal layers [claim 39].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zollo in view of US 2005/0039948 A1 (Asai).

Regarding claim 13, Zollo discloses the claimed invention as described above except Zollo does not specifically disclose that said interstitial bridge pad has a diameter in the range of from about 14 to 17 mils [claim 13]. However, it is well known in the art to form pads with a diameter in this range as evidenced by Asai ([0175]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to form the bridge pads in the invention of Zollo to have a diameter from about 14 to 17 mils as is known in the art and evidenced by Asai. The motivation

for doing so would have been to provide a pad that is sufficient in size to accommodate a blind via while not needlessly wasting space on the PCB.

Regarding claim 15, Zollo discloses the claimed invention as described above except Zollo does not specifically disclose that each of said first via and said second via has an aspect ratio of at least about 1:1 [claim 15]. However, it is well known in the art to form vias with an aspect ratio of at least about 1:1 as evidenced by Asai ([0173] and [0175]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to form the blind vias in the invention of Zollo with an aspect ratio of at least about 1:1 as is known in the art and evidenced by Asai. The motivation for doing so would have been to form via which may be formed with a tight center to center pitch.

Similarly, regarding claim 16, Zollo discloses the claimed invention as described above except Zollo does not specifically disclose that said interconnection unit has an effective aspect ratio of at least about 2:1 [claim 16]. However, it is well known in the art to form a double blind via interconnection unit with an aspect ratio of at least about 2:1 as evidenced by Asai ([0173] and [0175]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to form the interconnection unit in the invention of Zollo with an aspect ratio of at least about 2:1 as is known in the art and evidenced by Asai. The motivation for doing so would have been to form an interconnection unit which may be formed with a tight center to center pitch.

Regarding claim 17, Zollo discloses the claimed invention as described above including wherein: said first capture pad is located within a first conductive layer (6), said second capture pad is located within a second conductive layer (4), and said interconnection unit further comprises a third conductive layer (3). Zollo does not specifically disclose a third via extending from said first capture pad or said second capture pad to a third conductive layer. However, as evidenced by Asai (figure 6) it is well known in the art to supply a third via (52) to interconnect a second pad (24a2) to a third conductive layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to form a via to connect the second capture pad and the third conductive layer in the invention of Zollo as is known in the art and evidenced by Asai. The motivation for doing so would have been to allow for signal transmission between the second and third layers.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zollo in view of US 6,329,610 (Takubo).

Zollo discloses the claimed invention as described above except Zollo does not specifically disclose that said plurality of interstitial bridge pads are spaced apart from each other by a distance in the range of from about 0.7 to 4 mils [claim 24]. However, it is well known in the art to form pads spaced from each other a distance within the claimed range as evidenced by Takubo (col. 16, lines 30-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to form the pads in the invention of Zollo spaced apart from each other by a

distance in the range of from about 0.7 to 4 mils as is known in the art and evidenced by Takubo. The motivation for doing so would have been to form the pads with a tight pitch to avoid wasting board space. Moreover, the modified invention of Zollo teaches, wherein said plurality of interstitial bridge pads are arranged within said bridge layer at a center-to-center pitch in the range of from about 15 to 25 mils (Takubo col. 16, lines 30-45) [claim 25].

***Allowable Subject Matter***

Claims 1-4, 7, 8, 18-20, 40-57 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

**Regarding claims 1-4, 7, and 8**

Claim 1, and claims 2-4, 7, and 8 via dependency, state the limitations "wherein each of said plurality of interstitial bridge pads is coaxial in a z direction with said corresponding first blind via and with said corresponding second blind via" and "said corresponding first capture pad and said corresponding second capture pad each have a diameter less than a diameter of said interstitial bridge pad therebetween". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

**Regarding claims 18-20**

Claim 18, and claims 19-20 via dependency, state the limitations "wherein each pair of opposed coaxial blind vias in said dual blind via interconnection unit are coaxial "

and "each of said corresponding pairs of capture pads have a diameter less than a diameter of a corresponding one of said bridge pads". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

**Regarding claims 40-50**

Claim 40, and claims 41-50 via dependency, state the limitation "wherein said each of said bridge pad is coaxial in a z direction with a corresponding one of said first blind via and with a corresponding one of said second blind via" and "said corresponding first capture pad and said corresponding second capture pad each have a diameter less than a diameter of said bridge pad therebetween". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

**Regarding claims 51-54**

Claim 51, and claims 52-54 via dependency, state the limitations "wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via and wherein each of said interlayer interconnection units include coaxially formed corresponding first blind vias and second blind vias" and "said corresponding first capture pad and said corresponding second capture pad each have a diameter less than a diameter of said interstitial bridge pad therebetween". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

**Regarding claim 55**

Claim 55 states the limitations "wherein each pair of opposed coaxial blind vias in each of said plurality of interlayer interconnection units are coaxial, said pair of opposed coaxial blind vias extend from a corresponding pair of capture pads" and "each of said corresponding pairs of capture pads have a diameter less than a diameter of a corresponding one of said bridge pads". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

**Regarding claims 56-57**

Claim 56, and claim 57 via dependency, state the limitations "wherein each of said plurality of bridge pads is coaxial in a z direction with said first blind via and with said second blind via" and "said corresponding first capture pad and said corresponding second capture pad each have a diameter less than a diameter of said bridge pad therebetween". These limitations, in conjunction with the other claimed features, were neither found to be disclosed in, nor suggested by, the prior art.

***Response to Arguments***

Applicant's arguments with respect to claims 10, 12-17, 21, and 23-39 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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JCSN